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*DB=USPT; PLUR=YES; OP=ADJ*

<u>L7</u>	L6 and (interface near8 bus)	69	<u>L7</u>
<u>L6</u>	L5 and (bus near8 (clock or rate or timing or factor or ratio))	104	<u>L6</u>
<u>L5</u>	L4 and l3	157	<u>L5</u>
<u>L4</u>	L1 same (bus near4 (width or bandwidth or size or wide or capacity))	371	<u>L4</u>
<u>L3</u>	L2 same (bus near4 (width or bandwidth or size or wide or capacity))	5002	<u>L3</u>
<u>L2</u>	(memory or external) near8 bus	63758	<u>L2</u>
<u>L1</u>	(module or card or SIMM or DIMM) near8 (data near4 bus)	5959	<u>L1</u>

END OF SEARCH HISTORY

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*DB=USPT; PLUR=YES; OP=ADJ*

<u>L5</u>	L4 and (interface with bus)	48	<u>L5</u>
<u>L4</u>	L3 and (memory near4 control\$4)	73	<u>L4</u>
<u>L3</u>	L2 same L1 same (bus near4 (clock or speed or frequency or rate or bandwidth or width or wide))	79	<u>L3</u>
<u>L2</u>	memory near4 data near4 bus	20383	<u>L2</u>
<u>L1</u>	module near4 data near4 bus	2800	<u>L1</u>

END OF SEARCH HISTORY